



FIG. 2

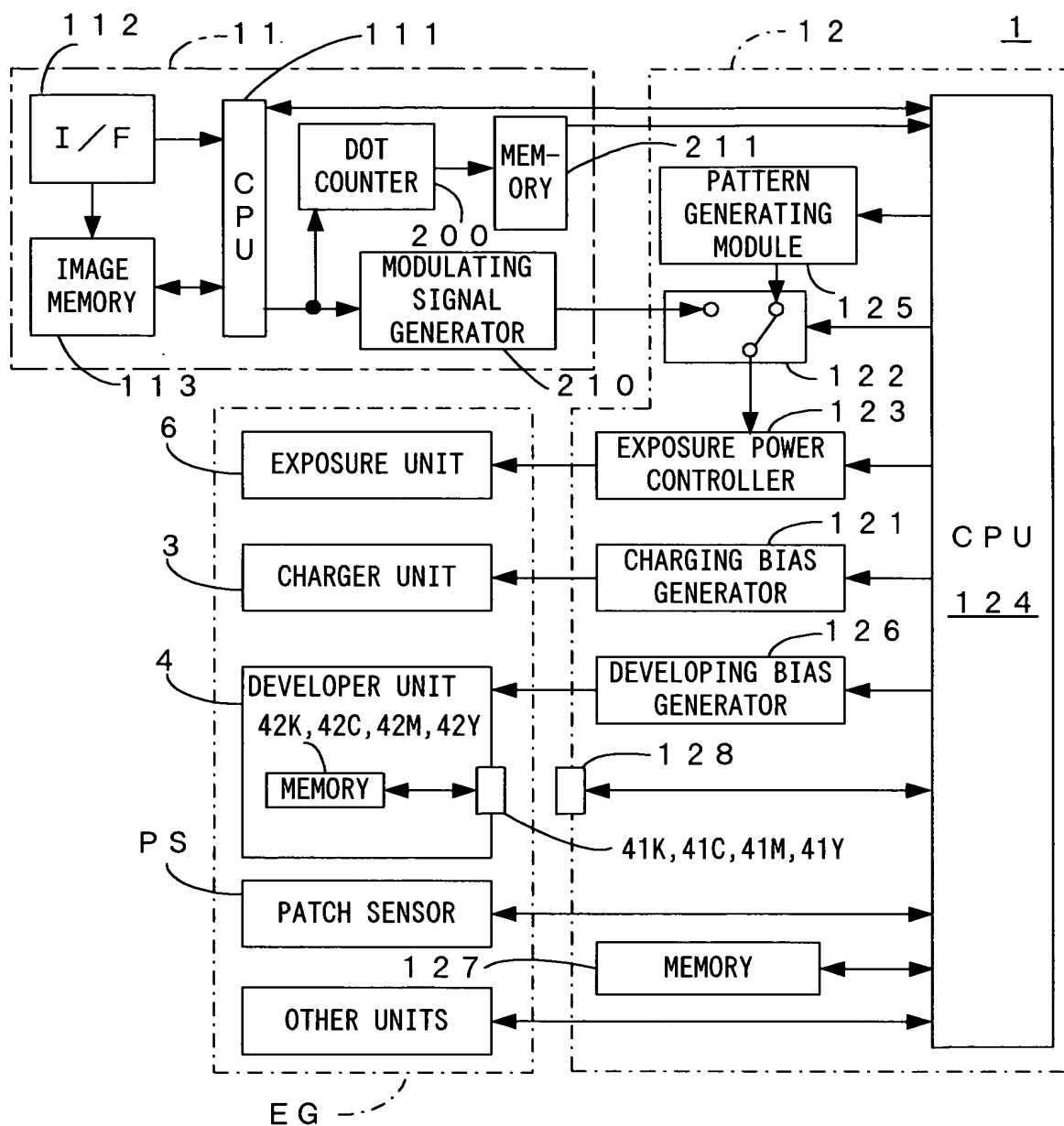


FIG. 3

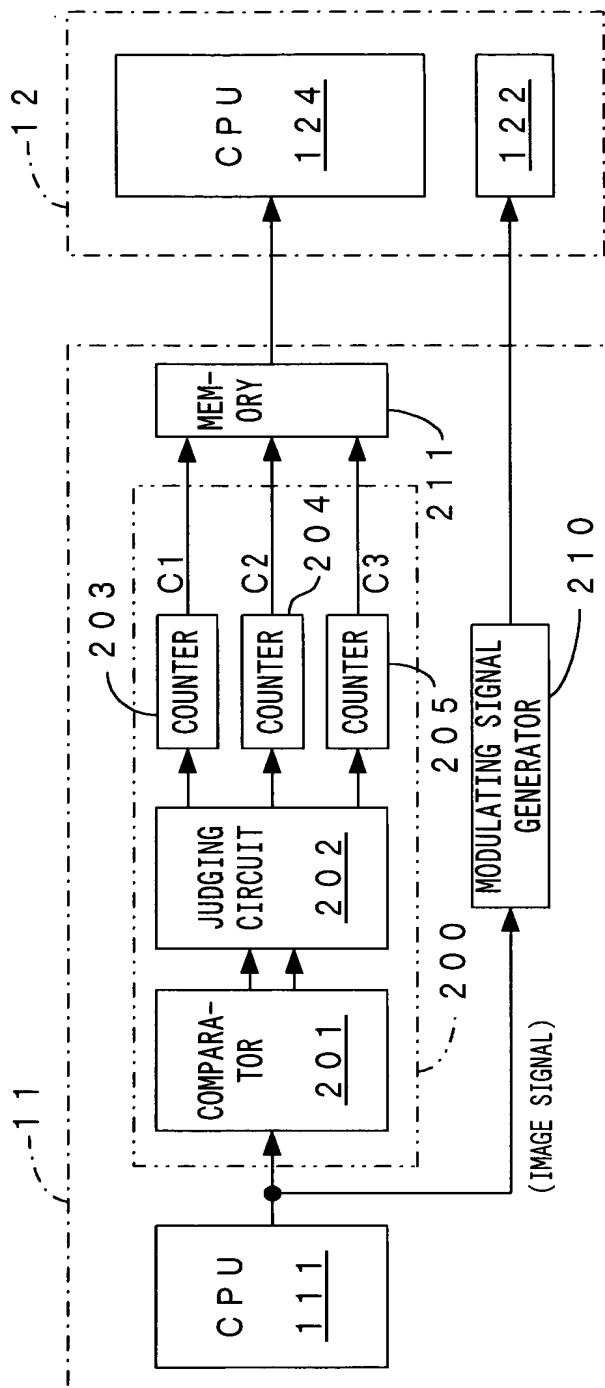


FIG. 4

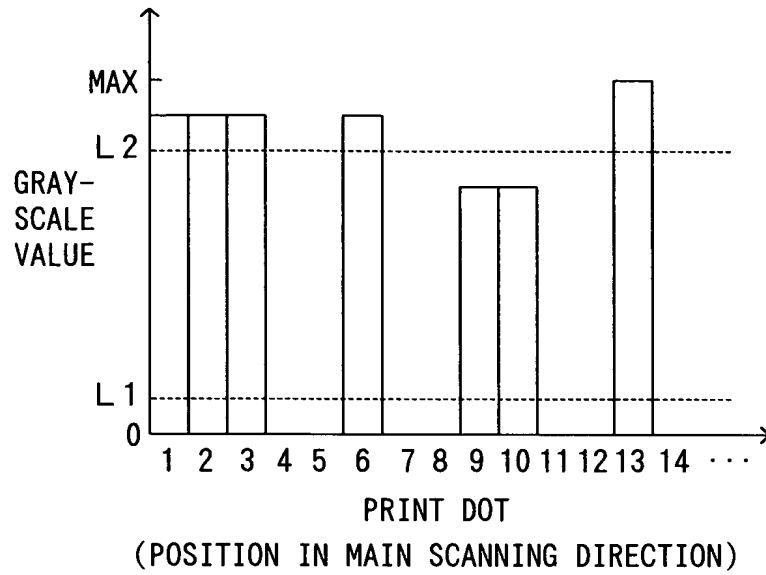


FIG. 5

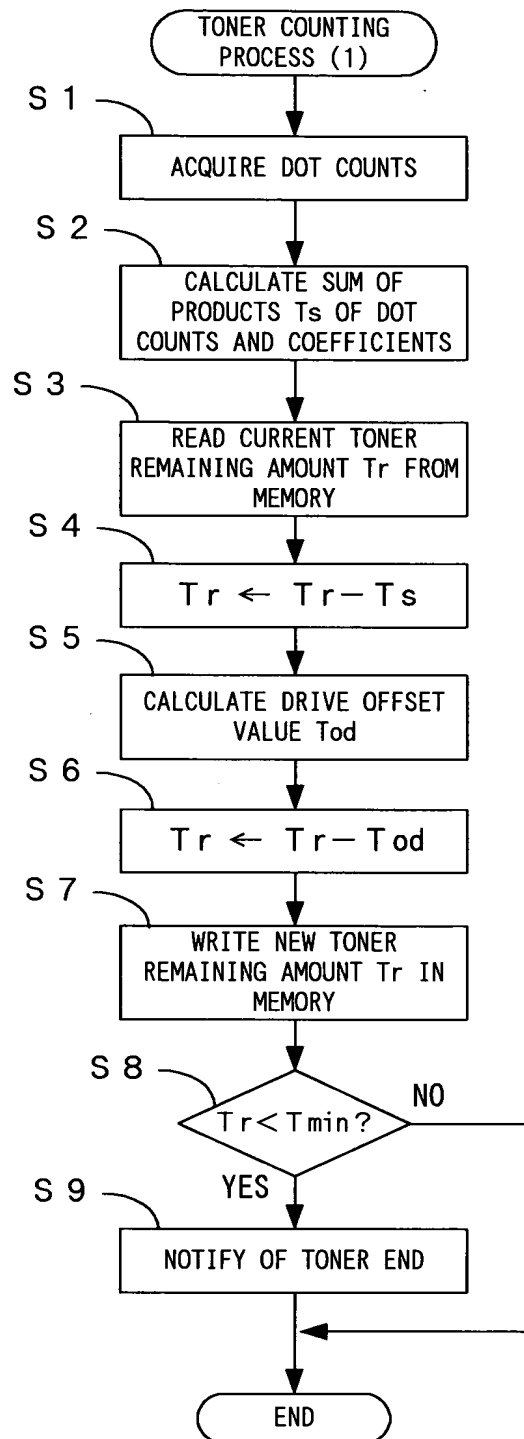


FIG. 6

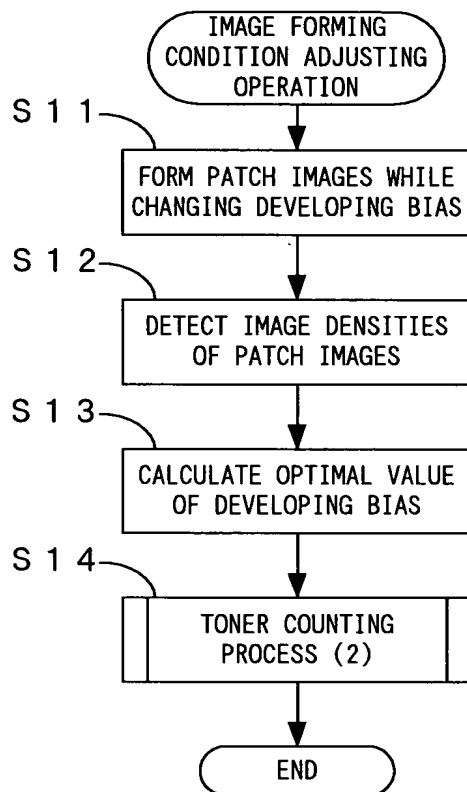


FIG. 7

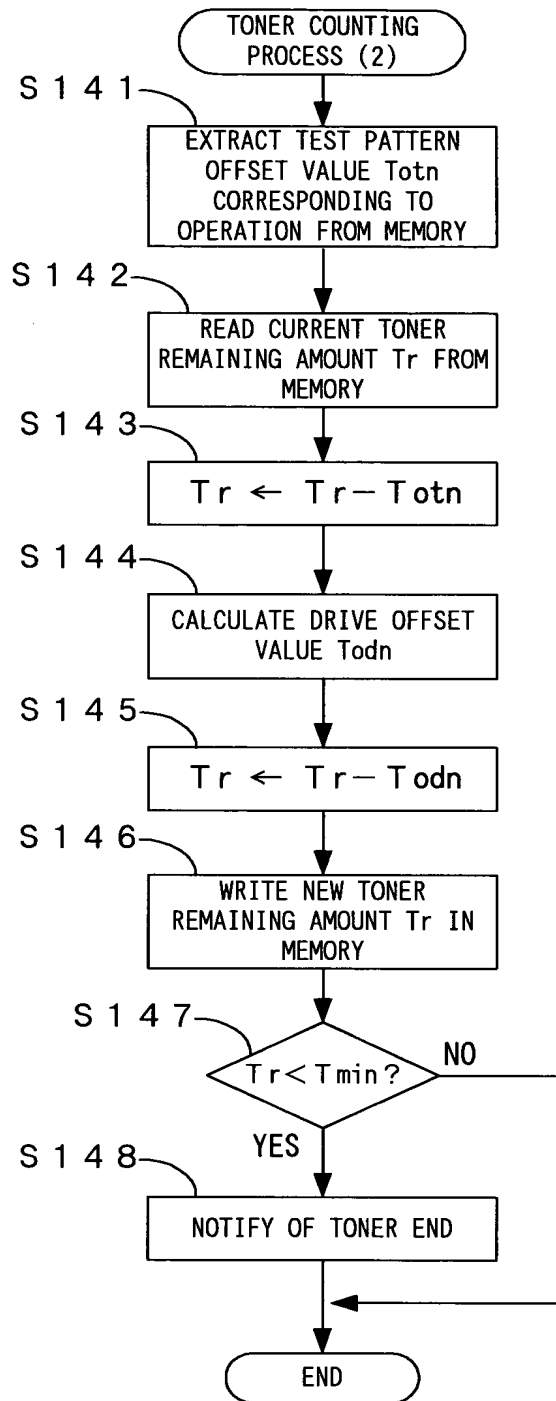


FIG. 8

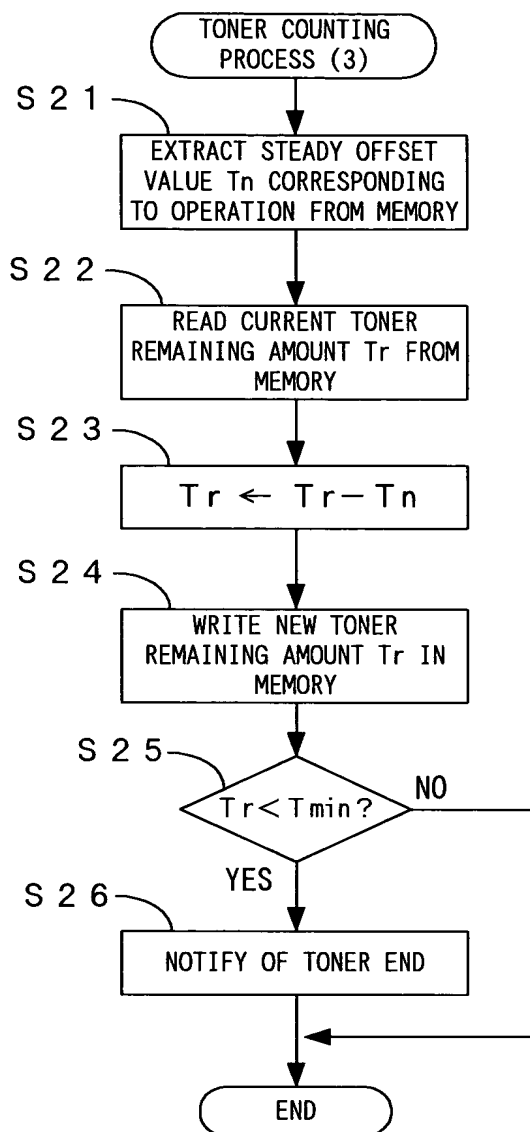




FIG. 9A

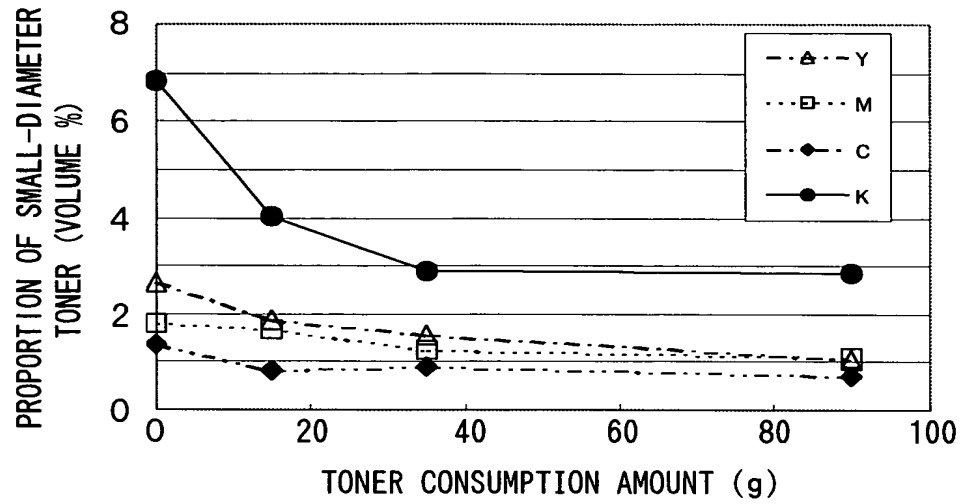
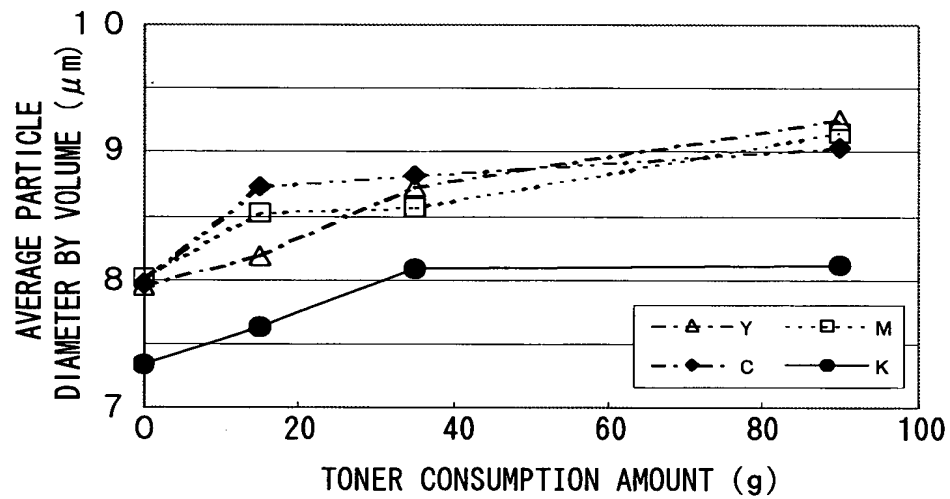


FIG. 9B



The diagram illustrates the architecture of a lithography system, centered around a CPU (111) and an I/F (112). The system is divided into several functional blocks and units, connected by various control and data lines.

**System Components and Connections:**

- 111 (CPU):** The central processing unit, connected to the I/F (112), Image Memory (113), DOT COUNTER (200), MODULATING SIGNAL GENERATOR (210), and PATTERN GENERATING MODULE (211).
- 112 (I/F):** Interface unit connected to the CPU (111) and Image Memory (113).
- 113 (IMAGE MEMORY):** Connected to the CPU (111) and I/F (112).
- 200 (DOT COUNTER):** Connected to the CPU (111) and MODULATING SIGNAL GENERATOR (210).
- 210 (MODULATING SIGNAL GENERATOR):** Connected to the CPU (111) and PATTERN GENERATING MODULE (211).
- 211 (PATTERN GENERATING MODULE):** Connected to the CPU (111) and EXPOSURE POWER CONTROLLER (123).
- 123 (EXPOSURE POWER CONTROLLER):** Connected to the CPU (111) and EXPOSURE UNIT (6).
- 121 (CHARGING BIAS GENERATOR):** Connected to the CPU (111) and CHARGER UNIT (3).
- 126 (DEVELOPING BIAS GENERATOR):** Connected to the CPU (111) and DEVELOPER UNIT (4).
- 128 (41K, 41C, 41M, 41Y):** Connected to the CPU (111) and DEVELOPER UNIT (4).
- 127 (MEMORY):** Connected to the CPU (111) and OTHER UNITS.
- 6 (EXPOSURE UNIT):** Connected to the EXPOSURE POWER CONTROLLER (123) and CHARGER UNIT (3).
- 3 (CHARGER UNIT):** Connected to the CHARGING BIAS GENERATOR (121) and DEVELOPER UNIT (4).
- 4 (DEVELOPER UNIT):** Contains a MEMORY (42K, 42C, 42M, 42Y) and is connected to the DEVELOPING BIAS GENERATOR (126) and 41K, 41C, 41M, 41Y (128).
- PS (PATCH SENSOR):** Connected to the DEVELOPER UNIT (4) and OTHER UNITS.
- OTHER UNITS:** Connected to the CPU (111) via the MEMORY (127) and the PATCH SENSOR (PS).

The diagram also shows various control and data lines (e.g., 111, 112, 113, 200, 210, 211, 123, 121, 126, 128, 127, 41K, 41C, 41M, 41Y) connecting the components.

FIG. 11

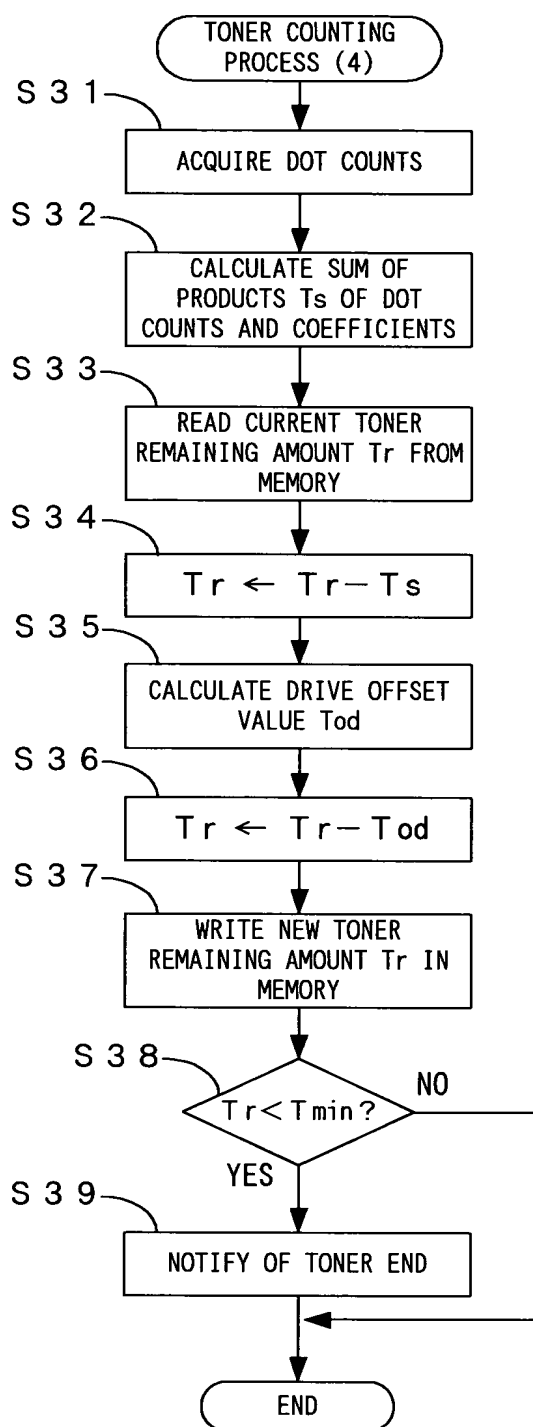


FIG. 12

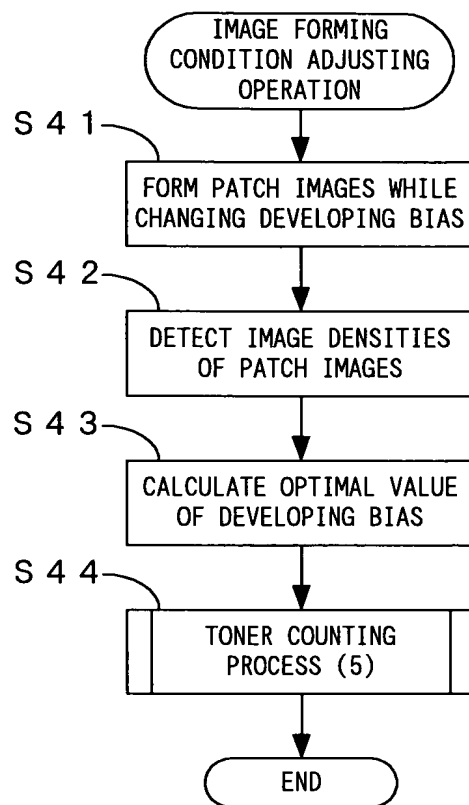


FIG. 13

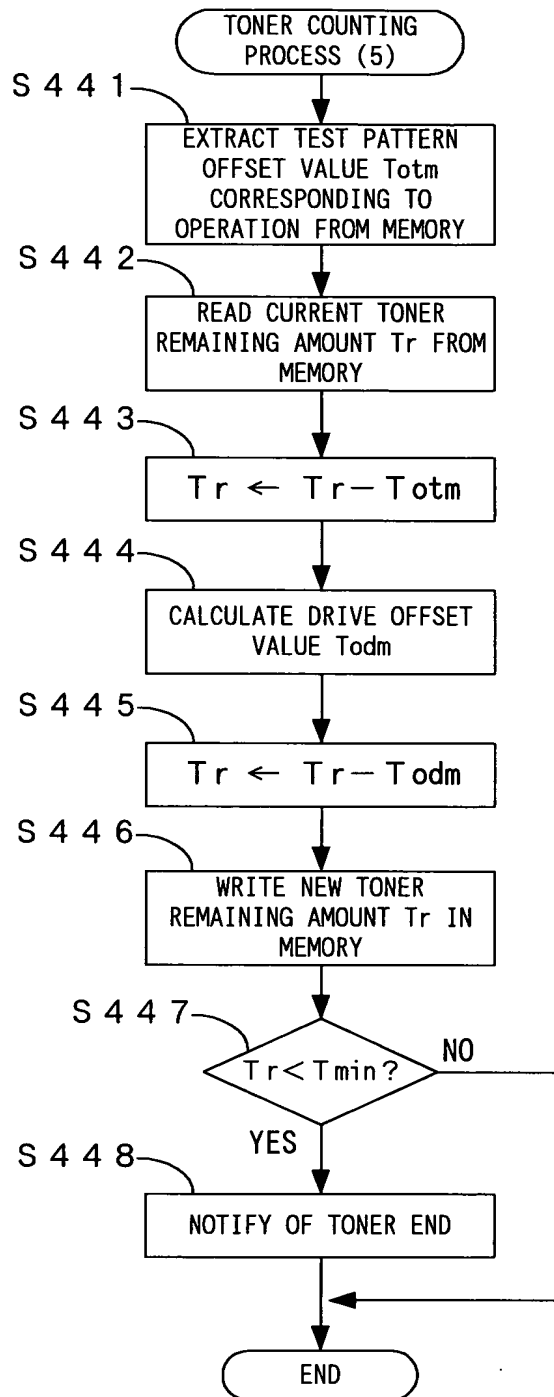


FIG. 14

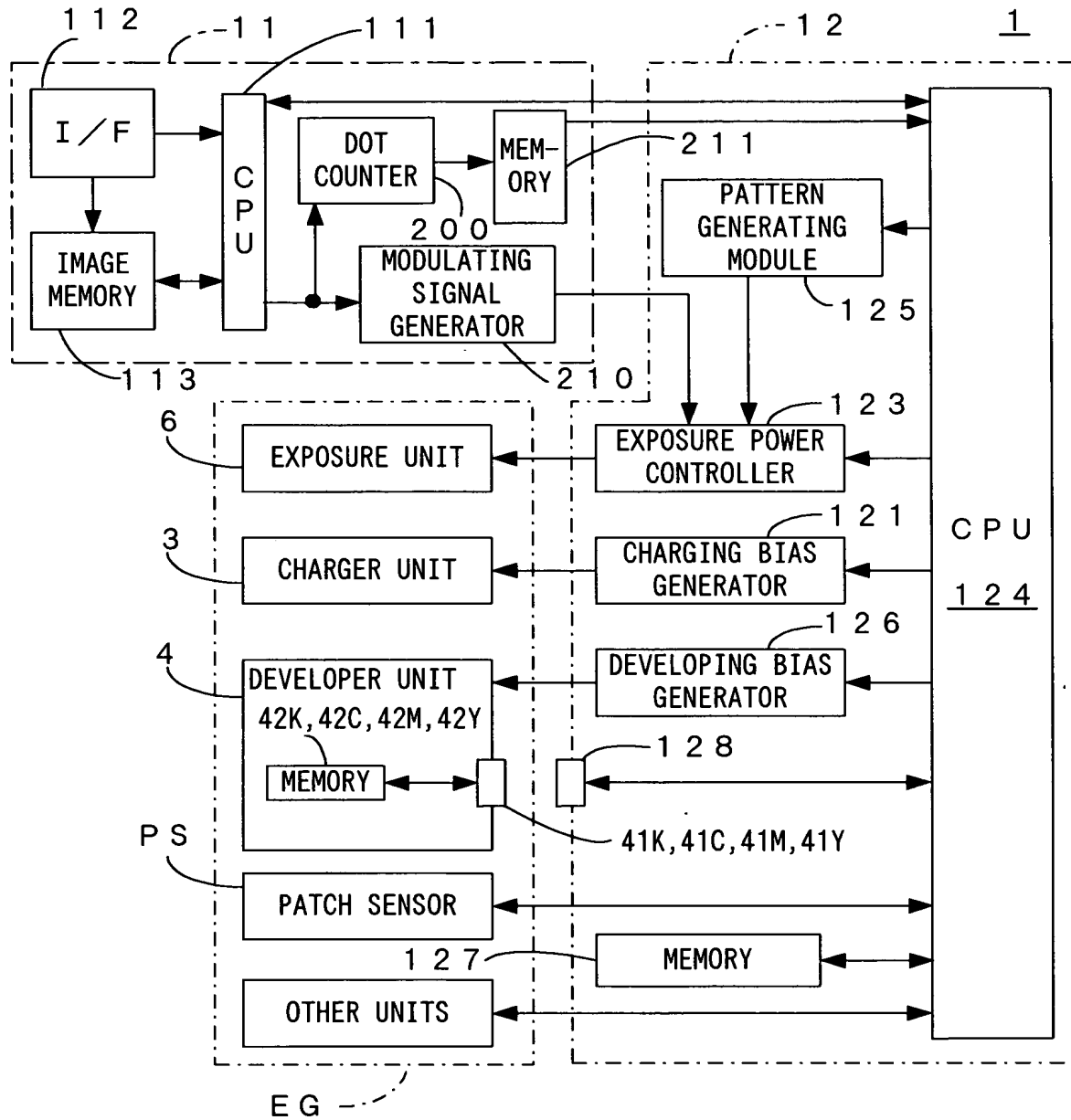


FIG. 15A

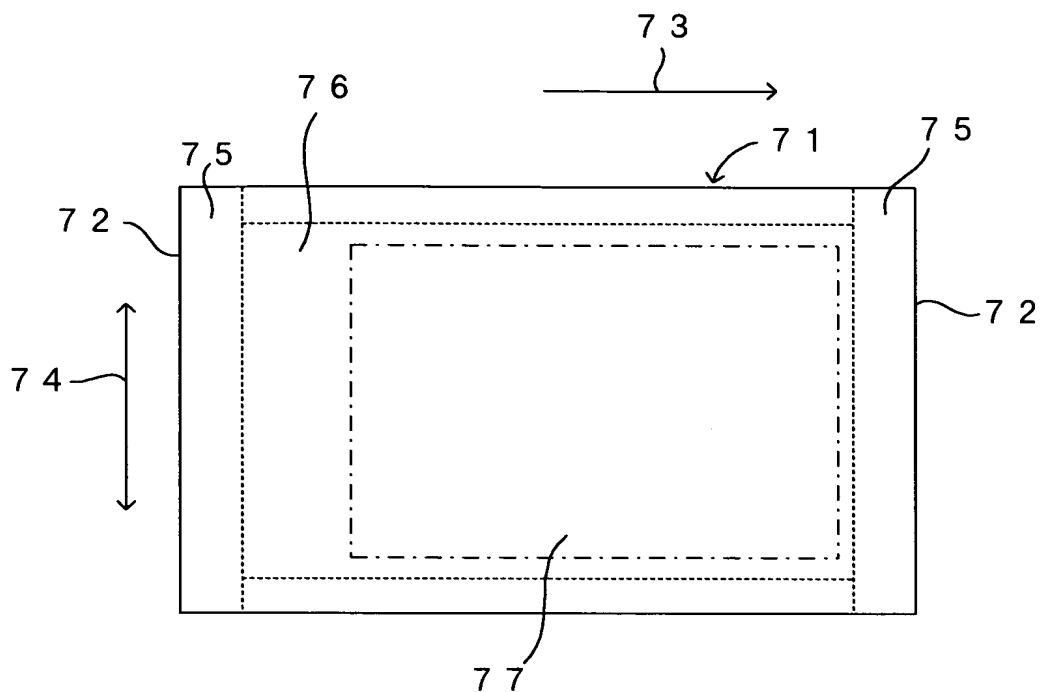


FIG. 15B

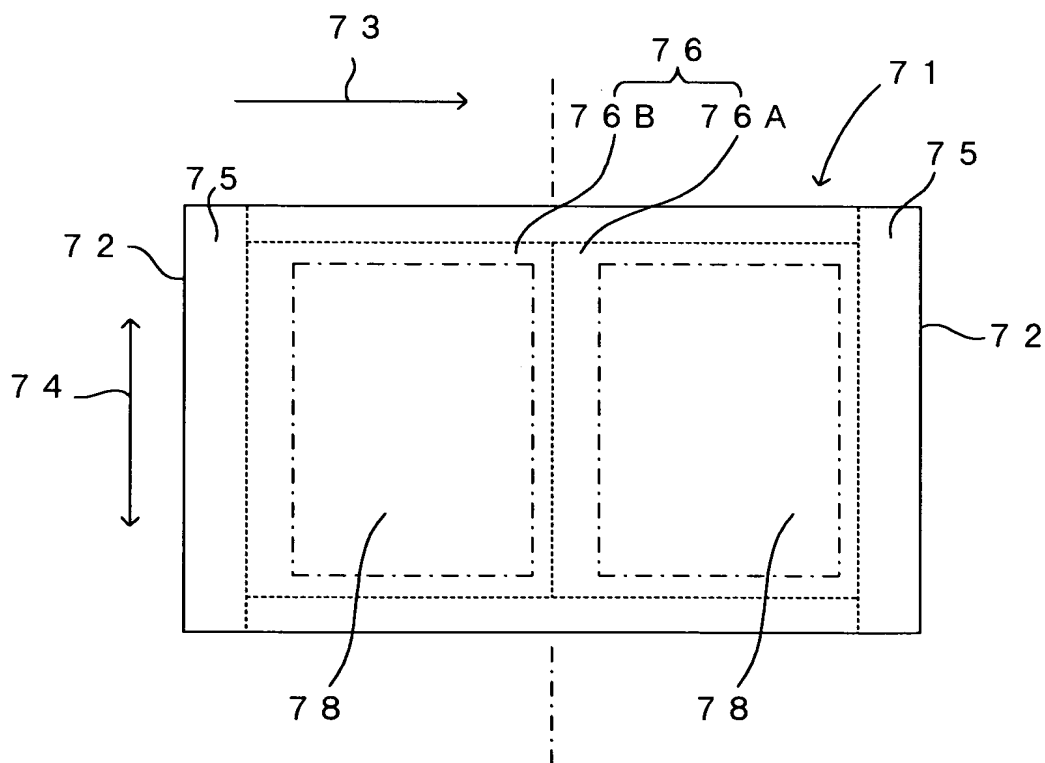


FIG. 16

| OFFSET VALUE TABLE DATA     |         | ONE OF<br>TWO PAGES | OTHERS |
|-----------------------------|---------|---------------------|--------|
| HIGH IMAGE-<br>QUALITY MODE | O H P   | T 1 1               | T 1 5  |
|                             | NON-OHP | T 1 2               | T 1 6  |
| TONER SAVE<br>MODE          | O H P   | T 1 3               | T 1 7  |
|                             | NON-OHP | T 1 4               | T 1 8  |



FIG. 17

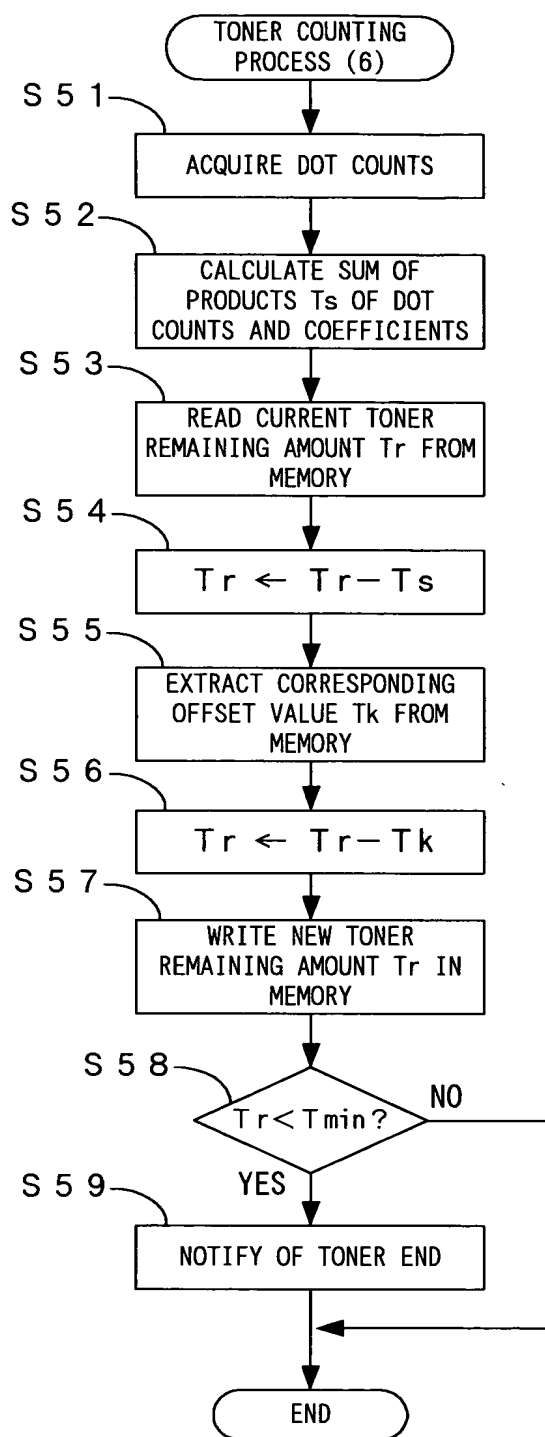


FIG. 18

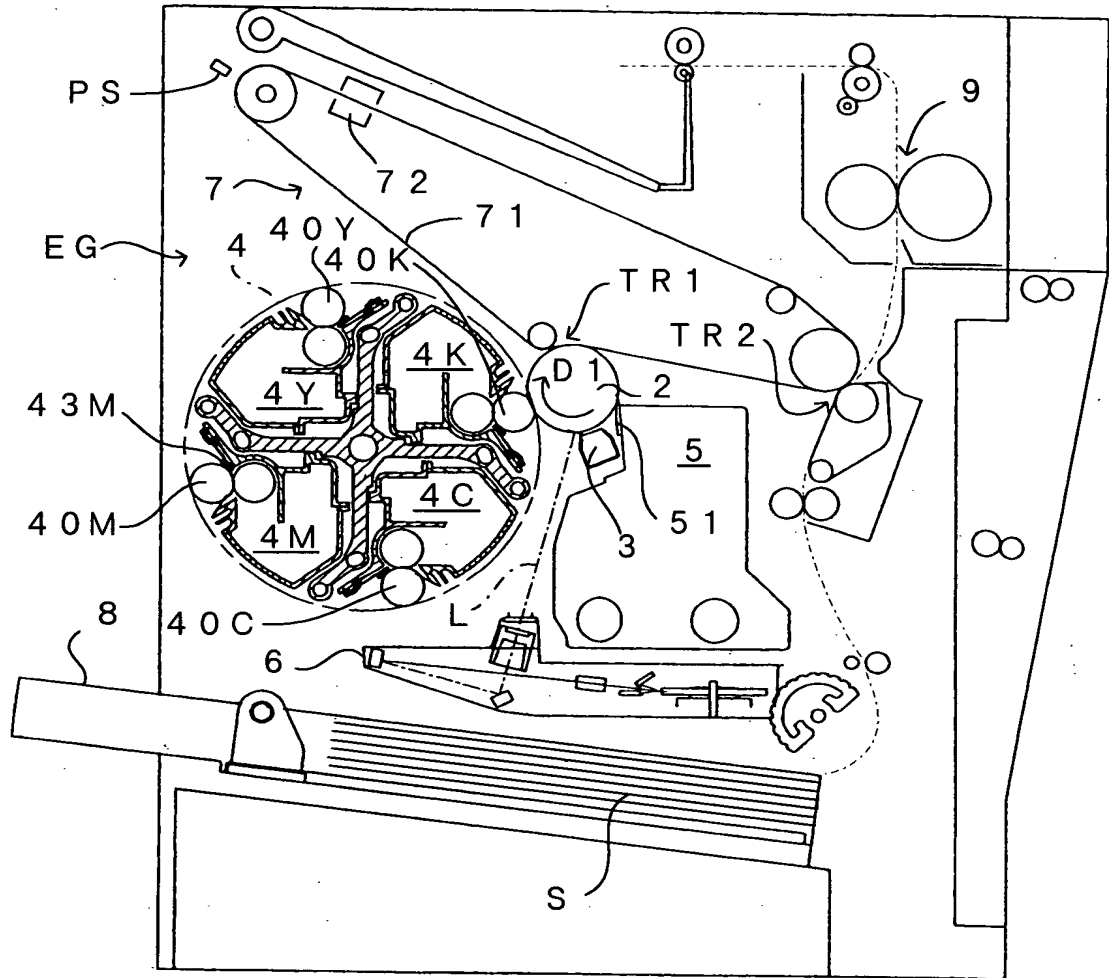


FIG. 19

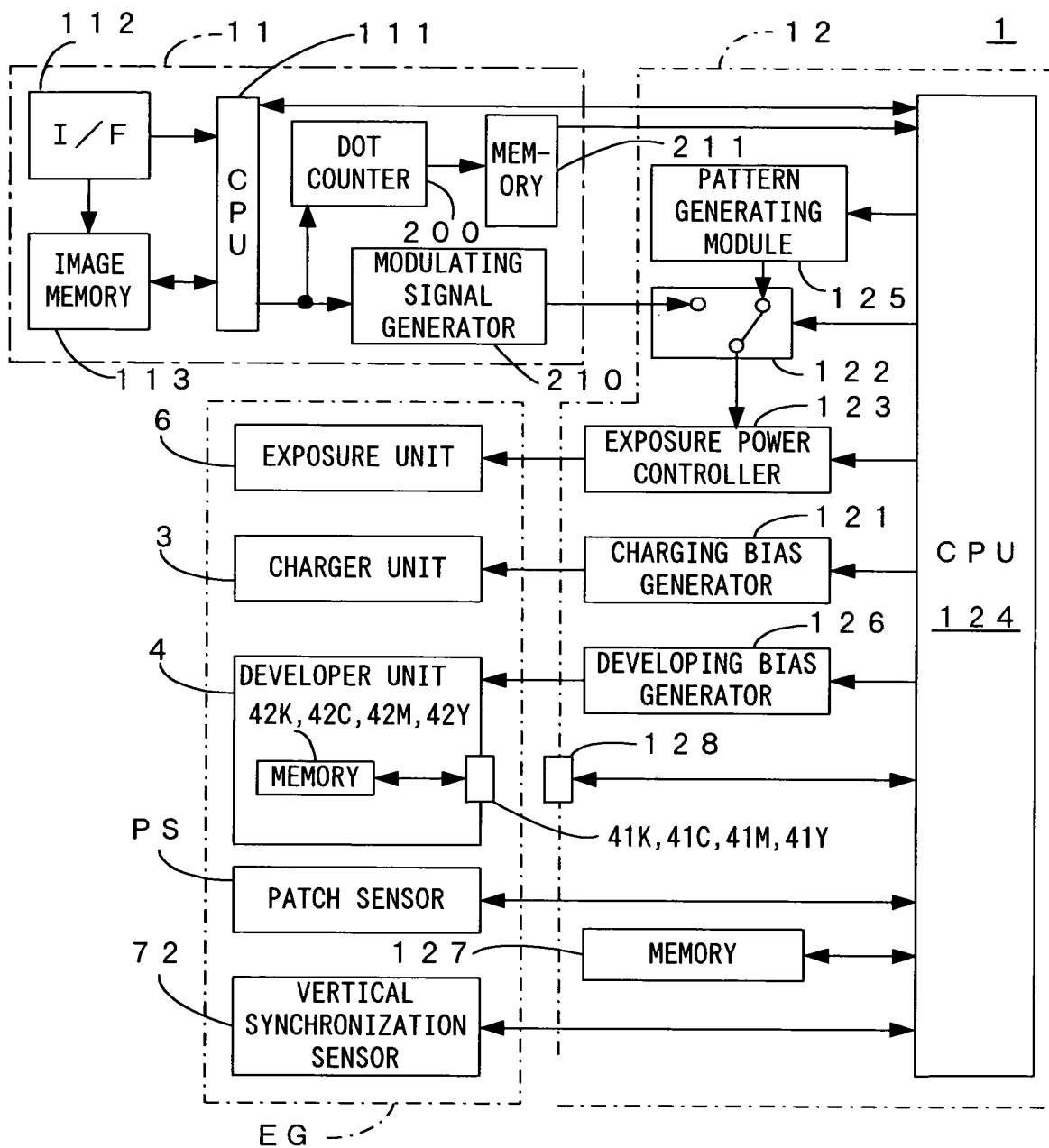


FIG. 20

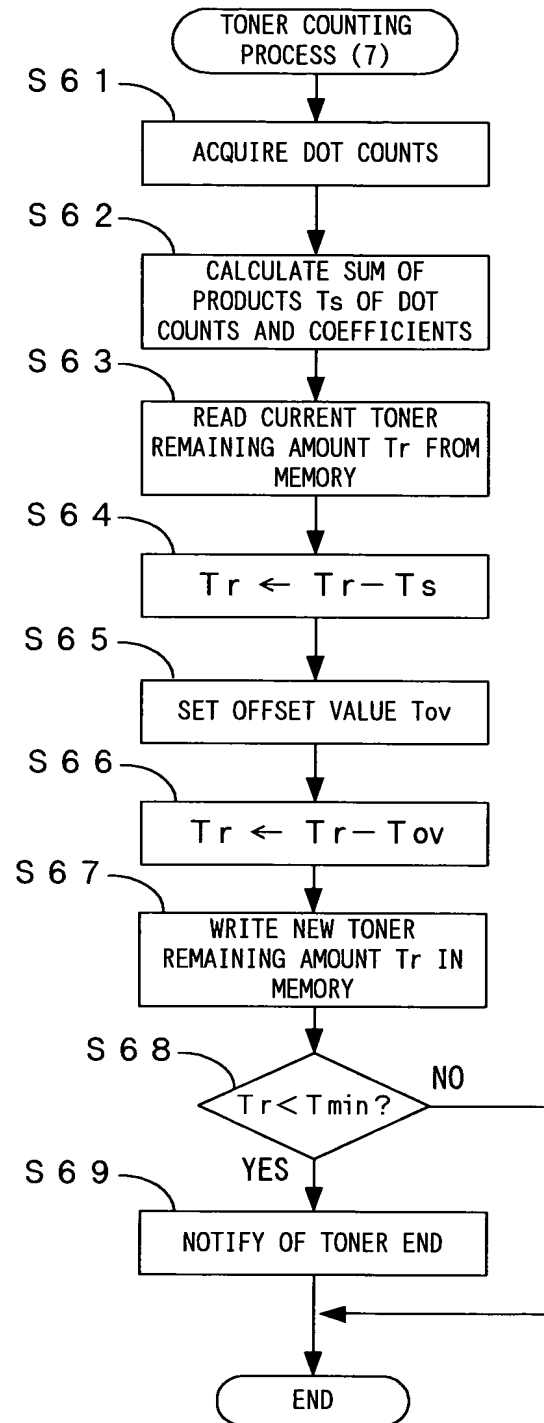


FIG. 21A

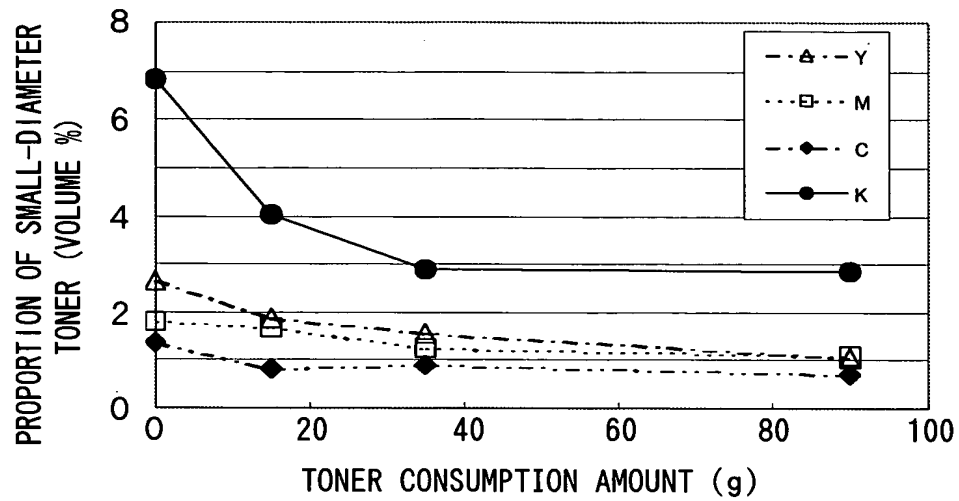


FIG. 21B

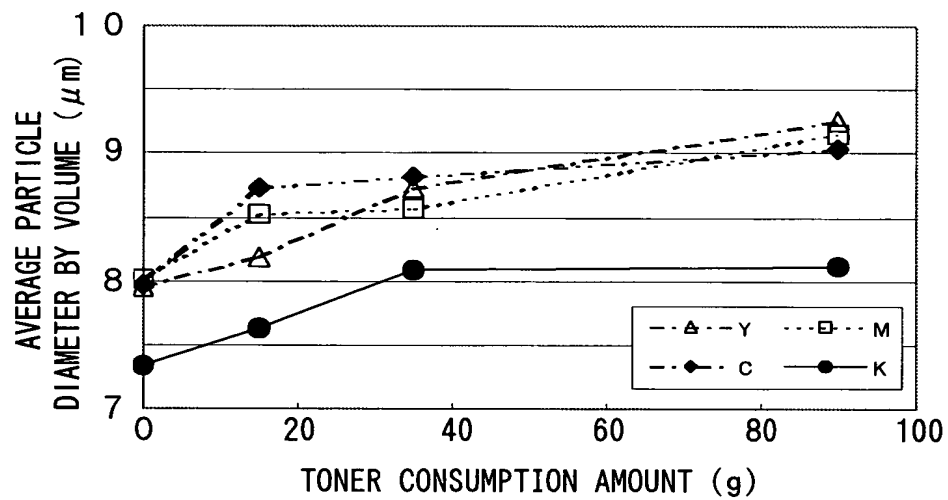


FIG. 22

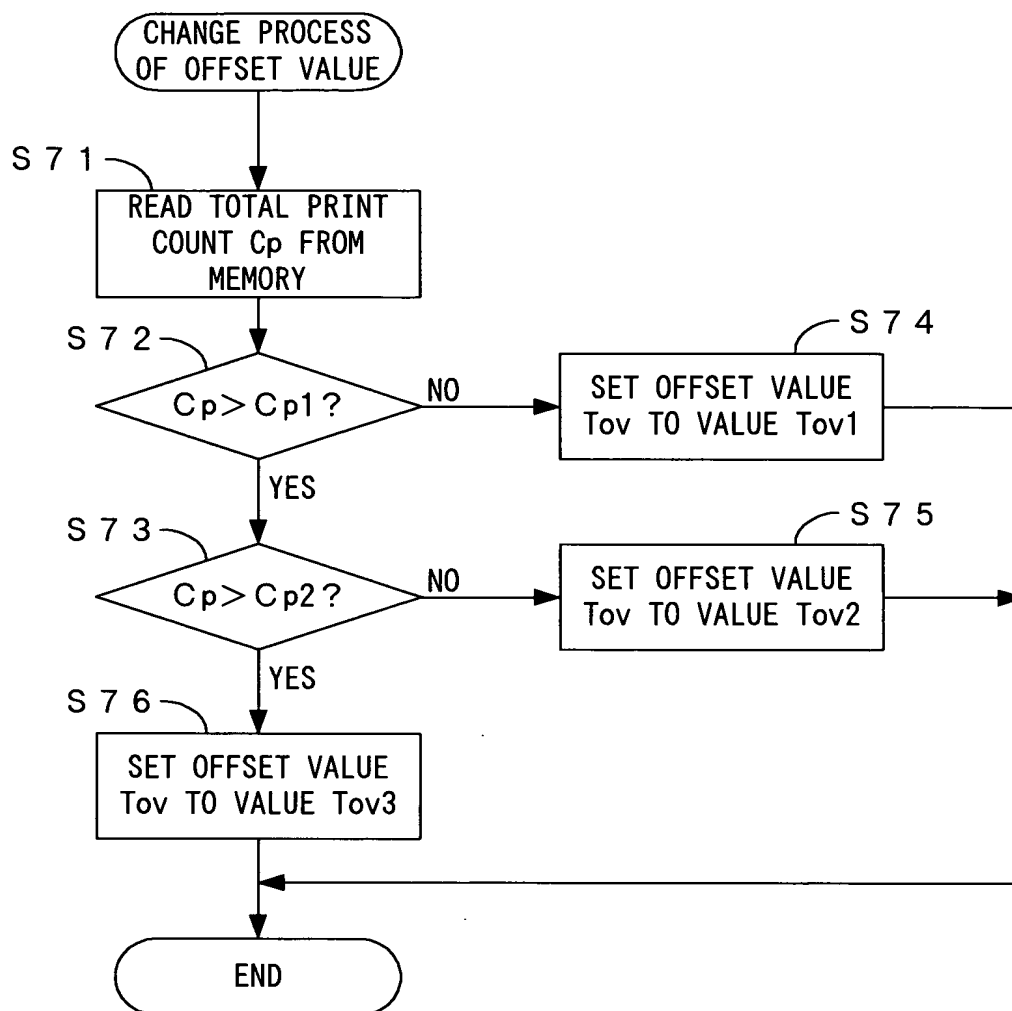


FIG. 23

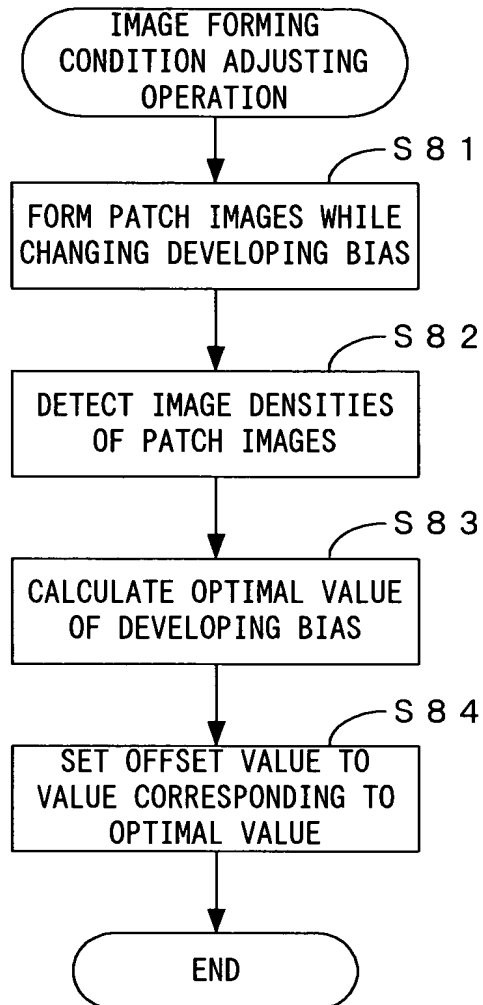


FIG. 24

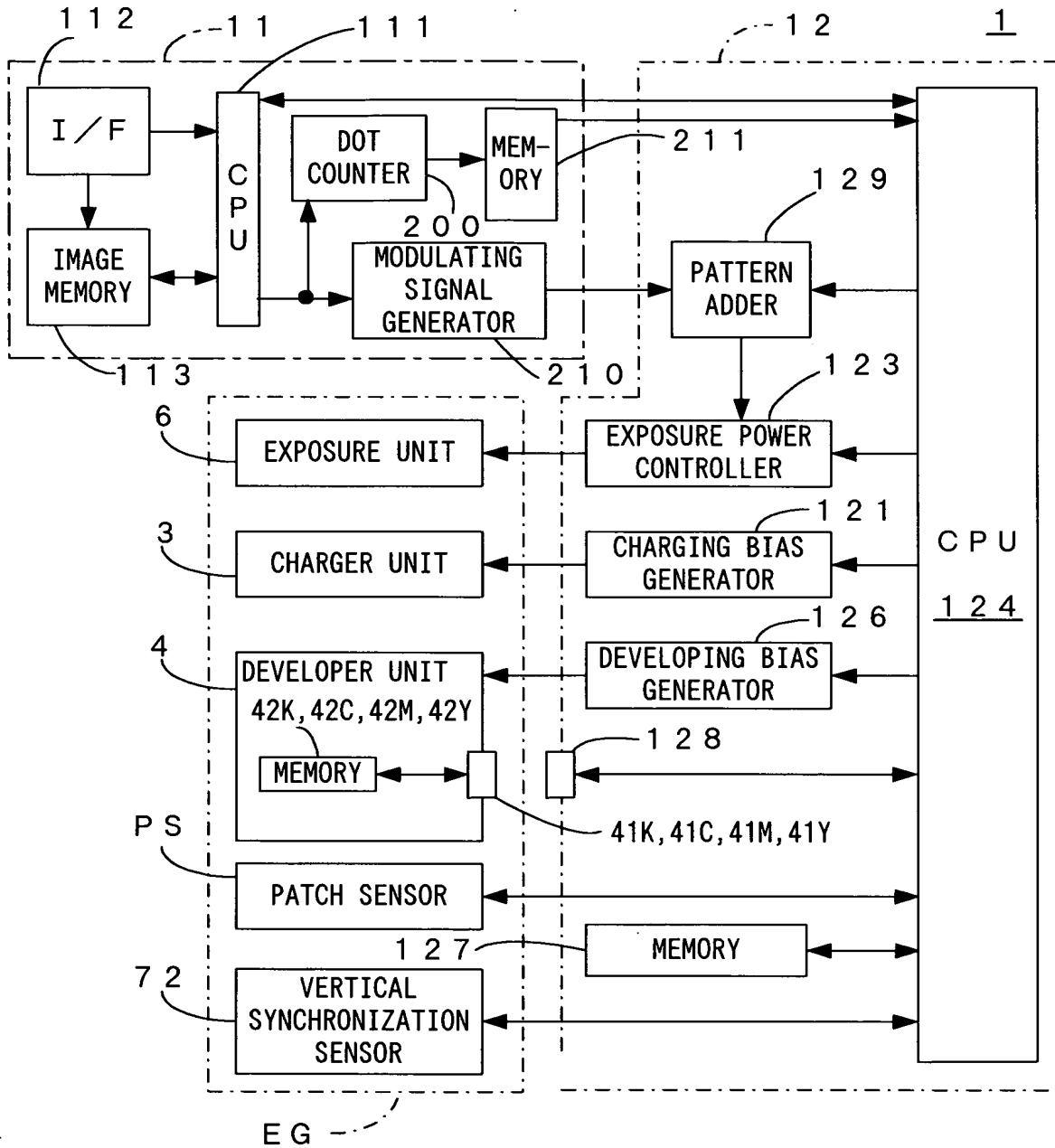




FIG. 25

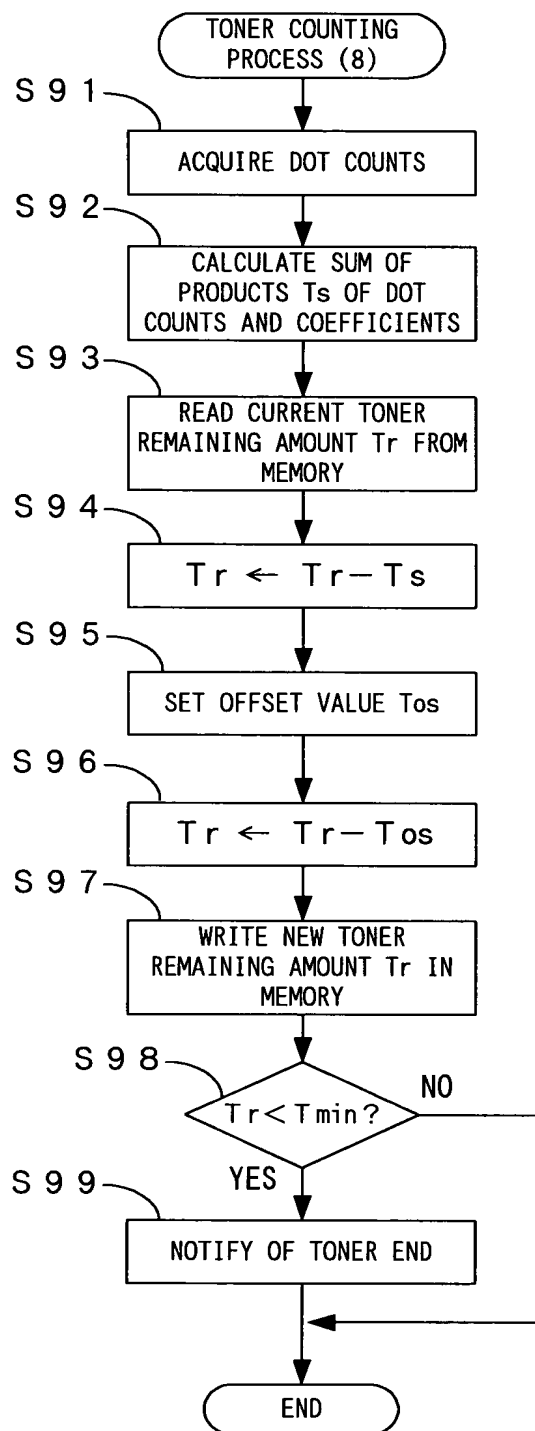
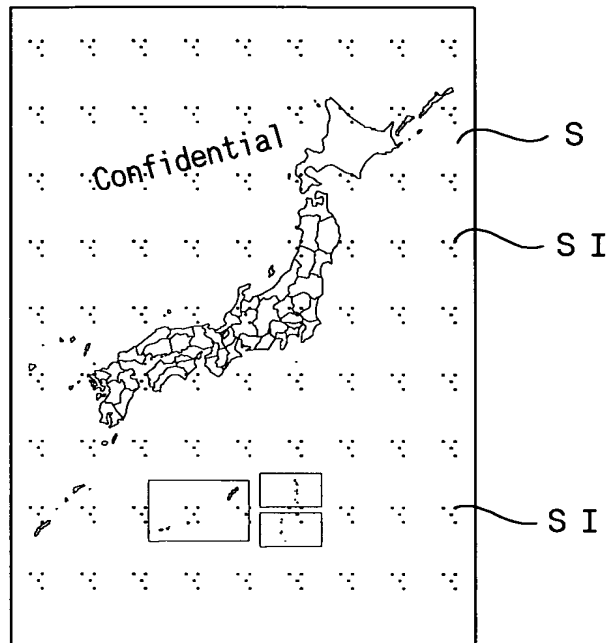


FIG. 26



BACKGROUND ART